

FIG. 1A

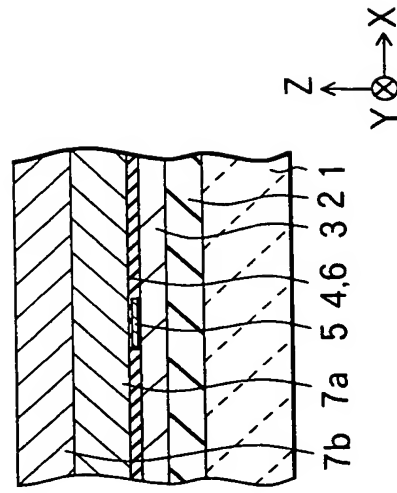


FIG. 1B

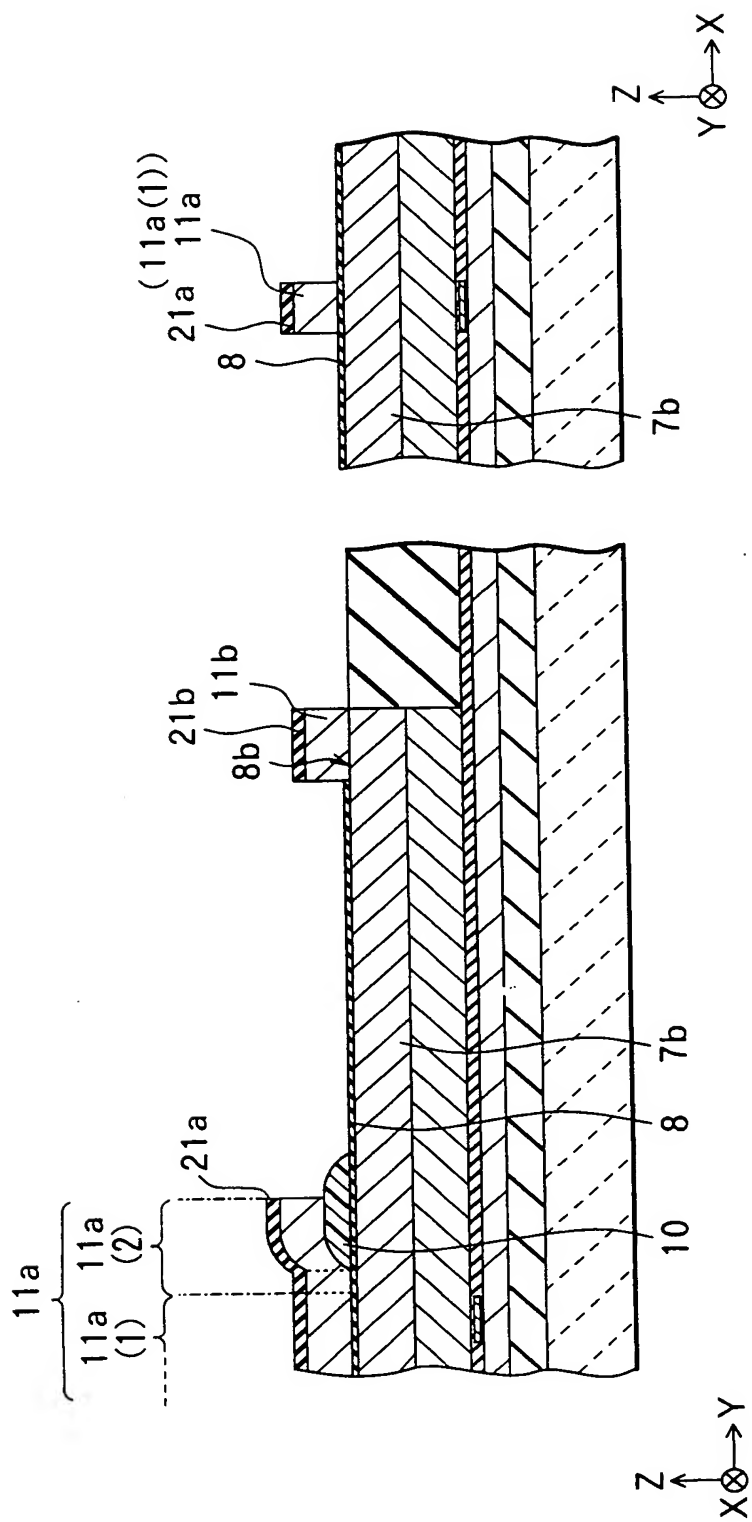


FIG.2A

FIG.2B

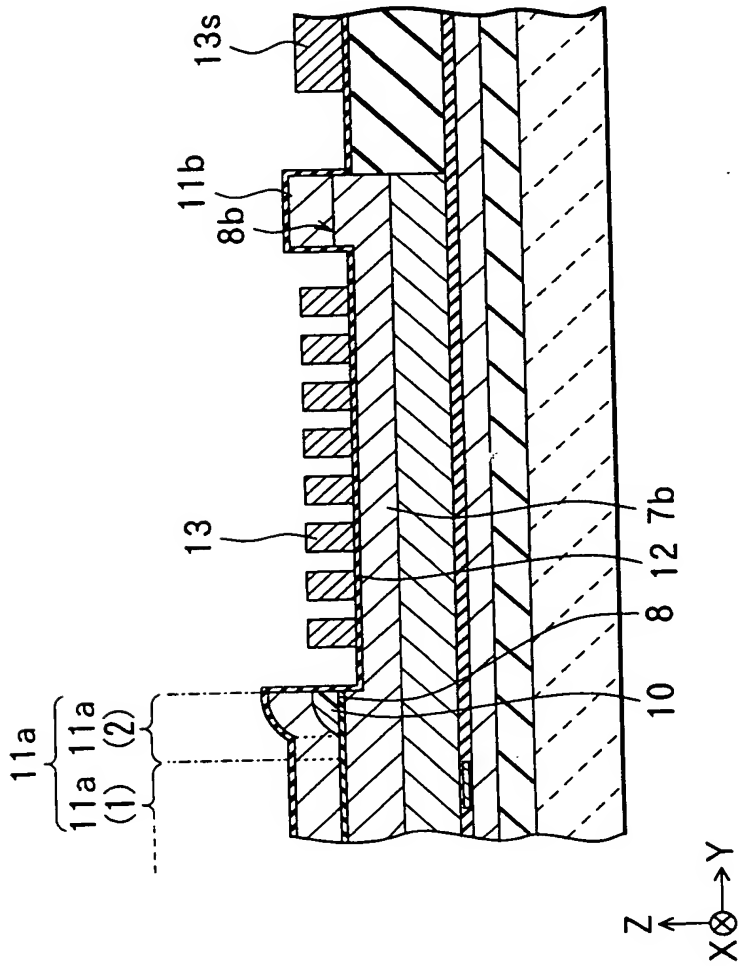


FIG.3A

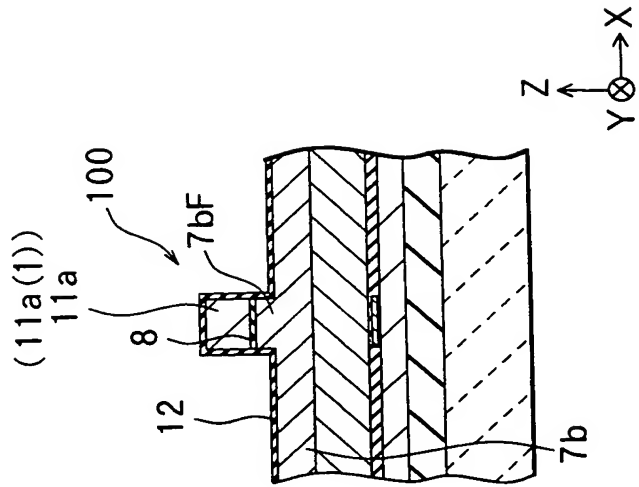


FIG.3B

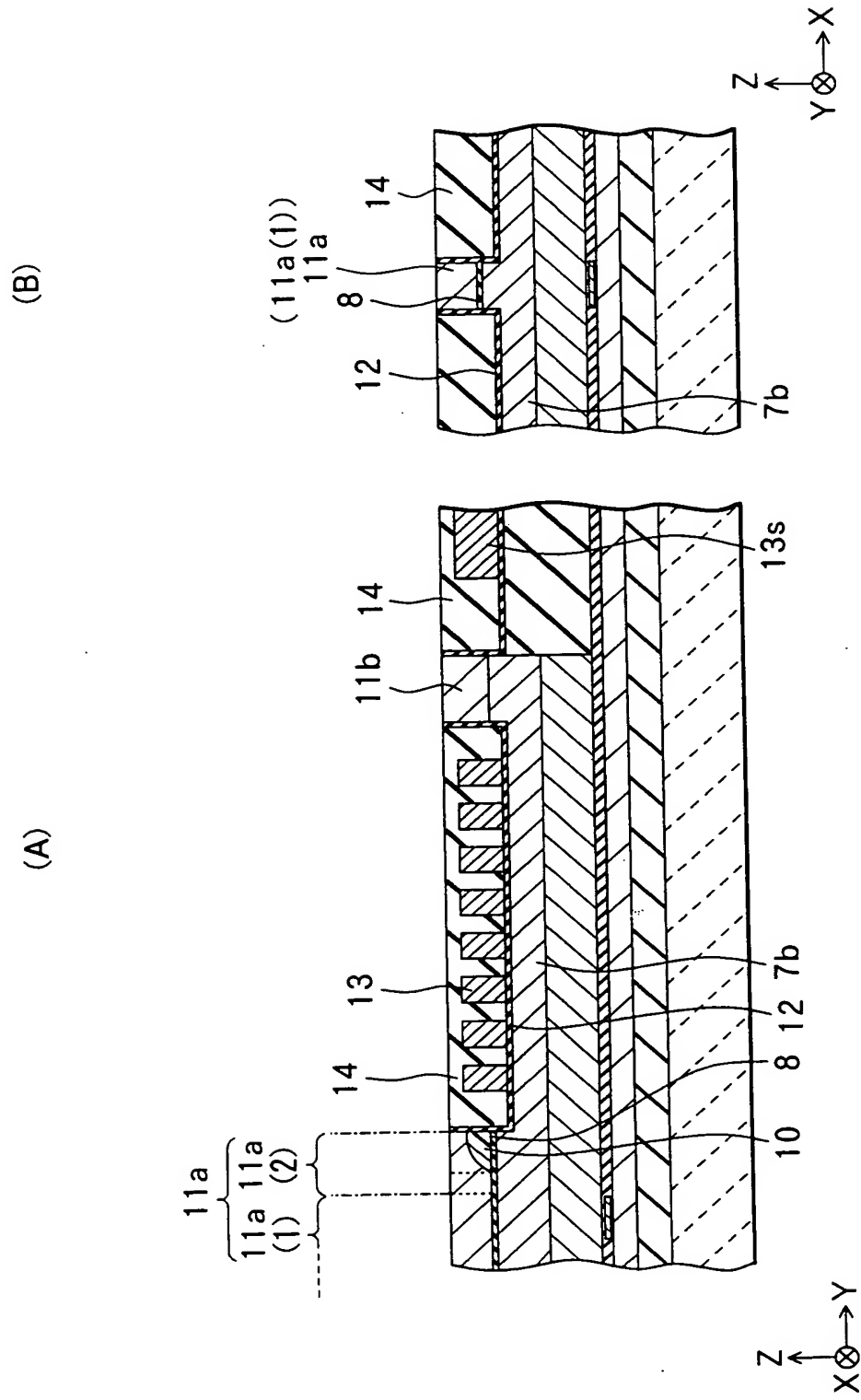


FIG. 4B

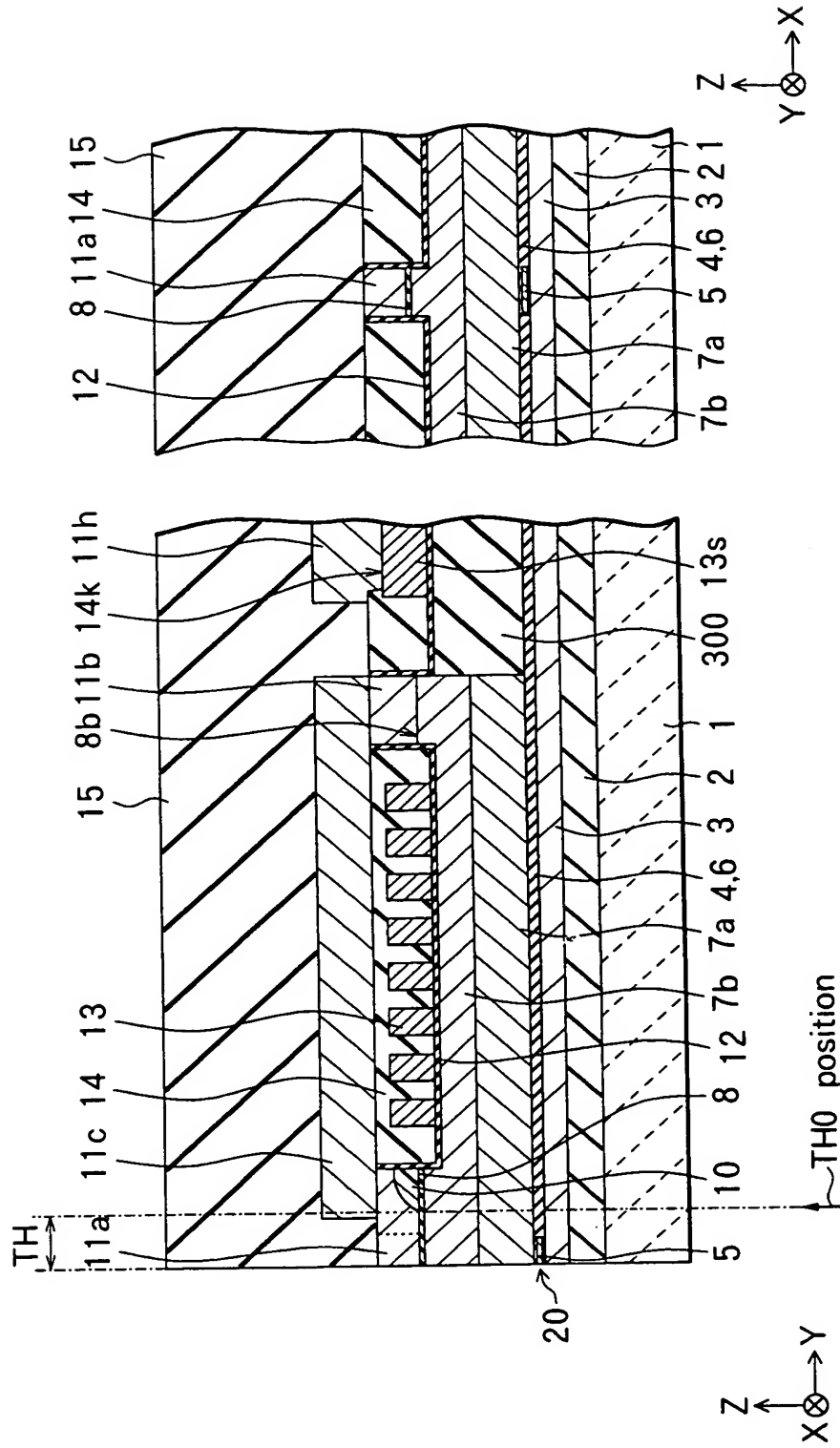


FIG.5B

FIG.5A

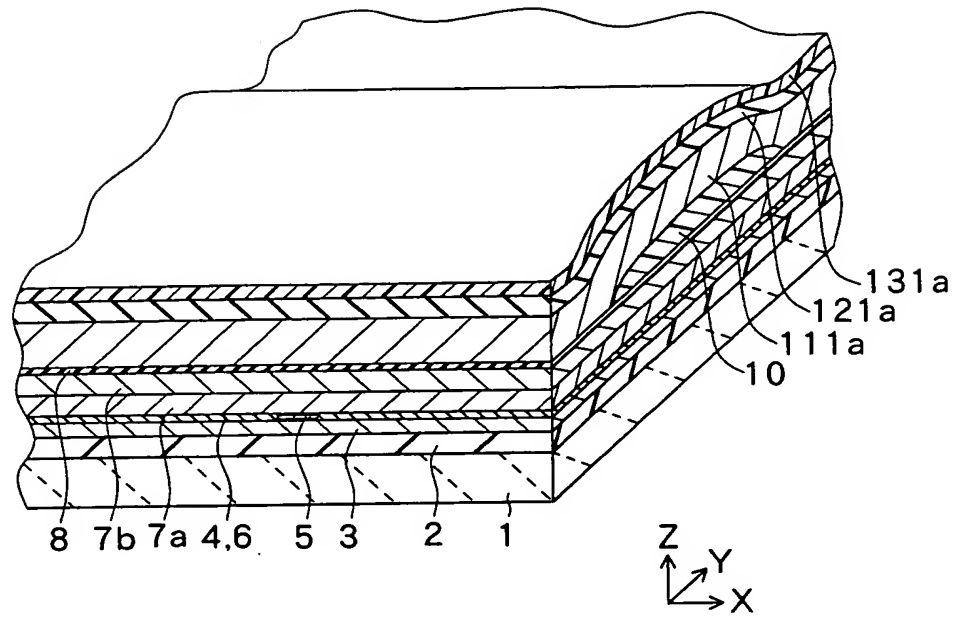


FIG. 6

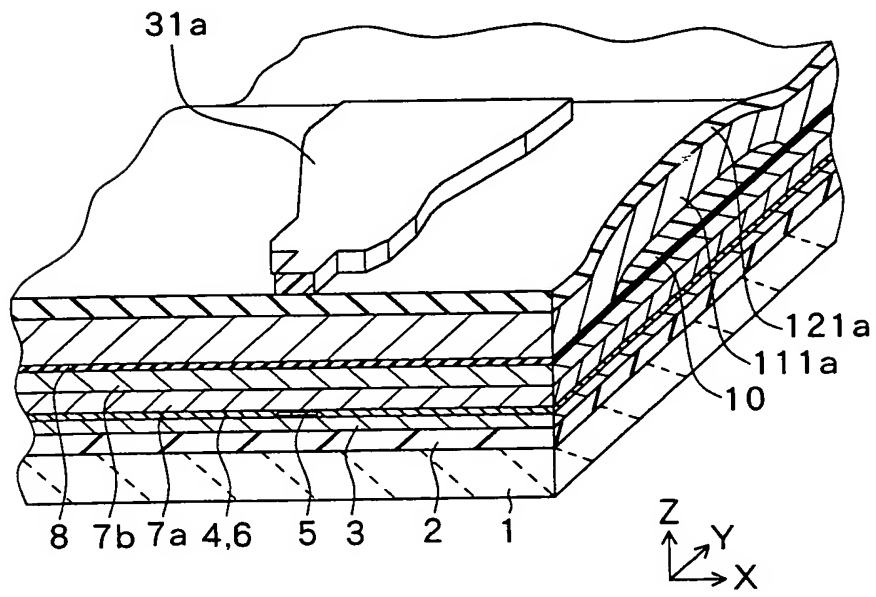


FIG. 7

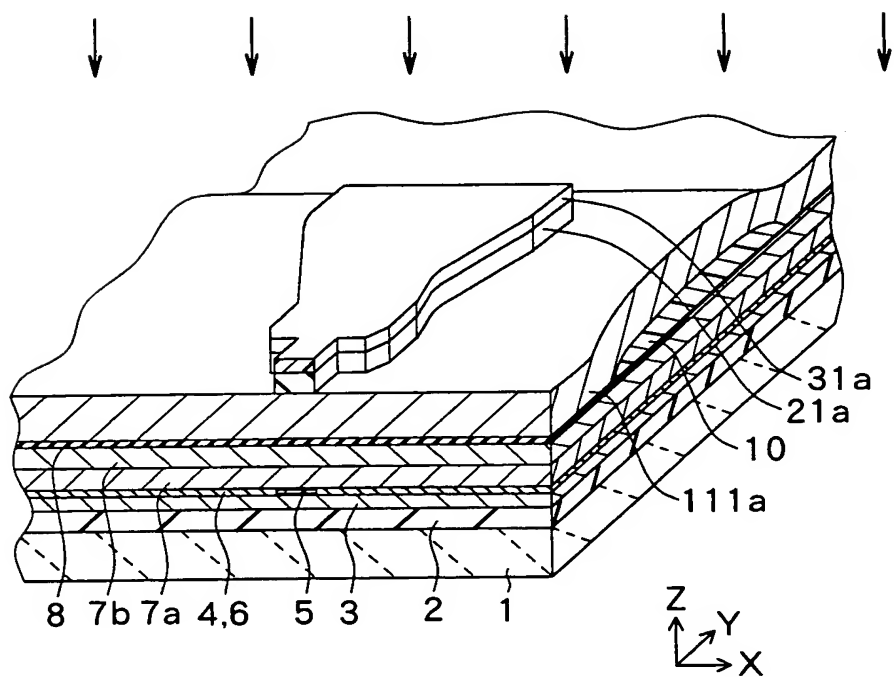


FIG. 8

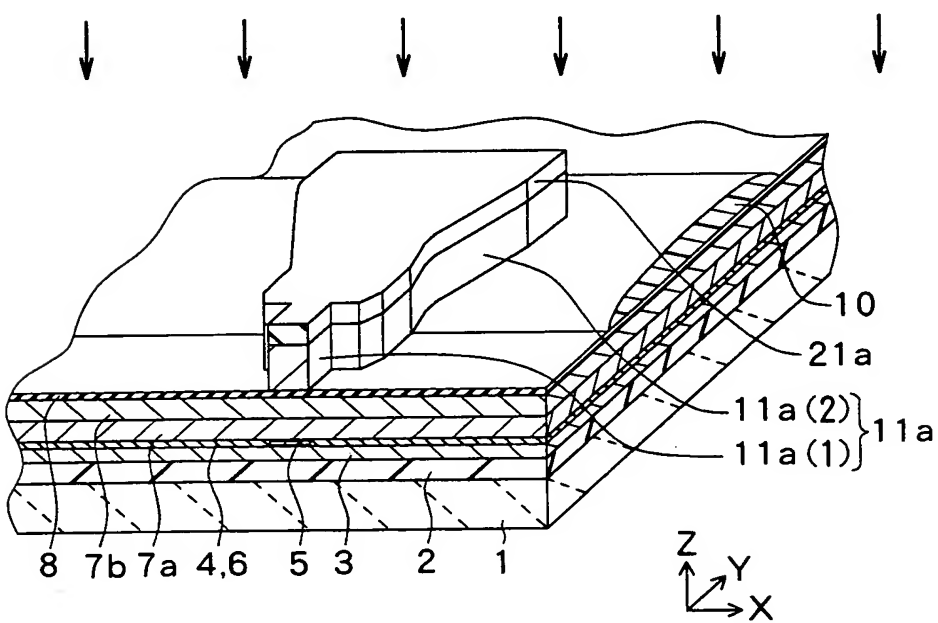


FIG. 9

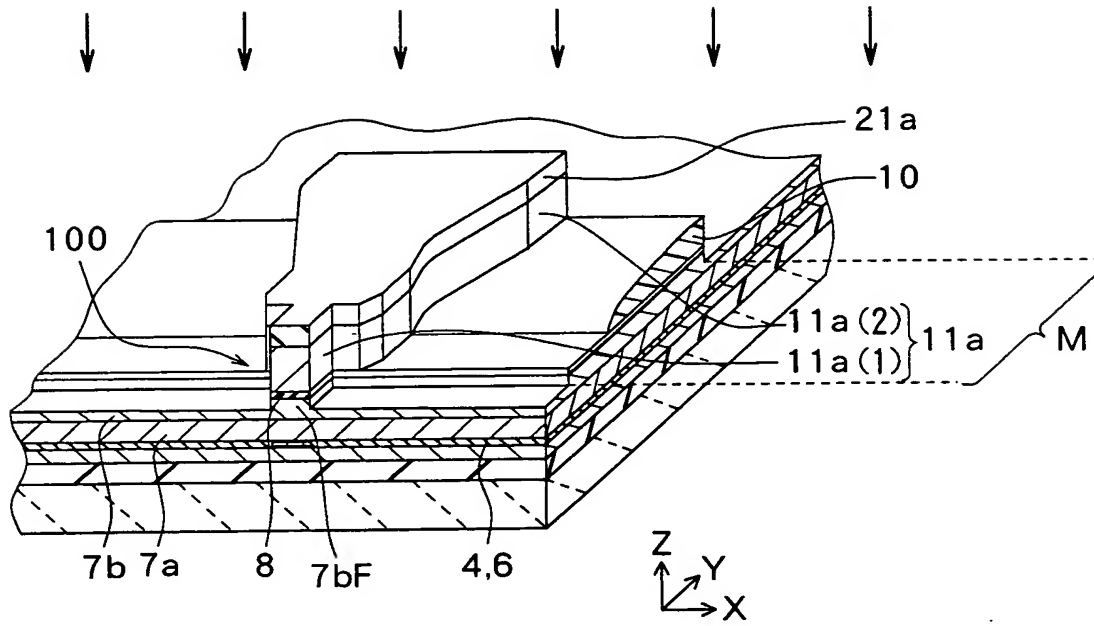


FIG.10

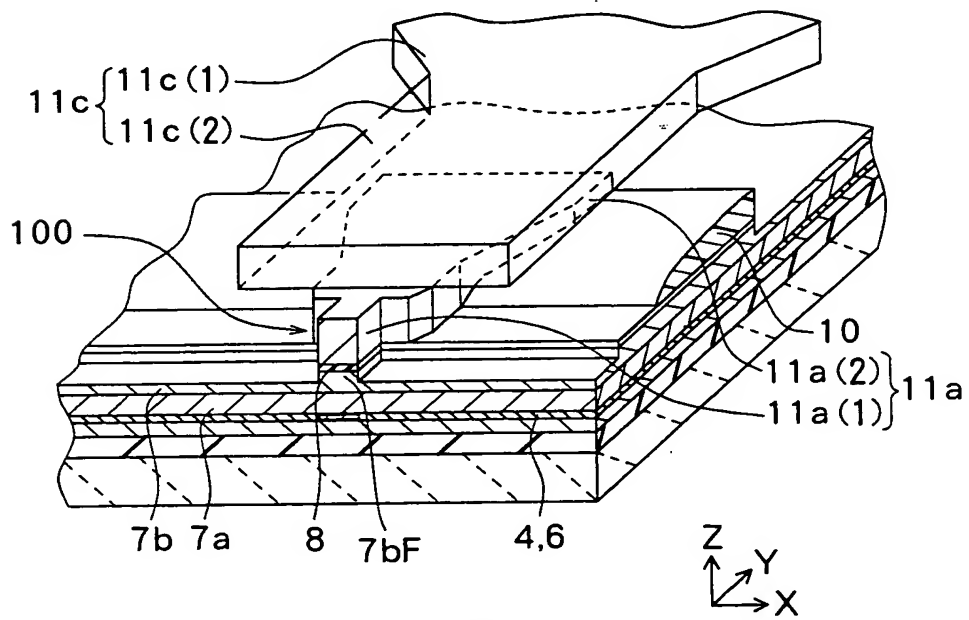


FIG.11

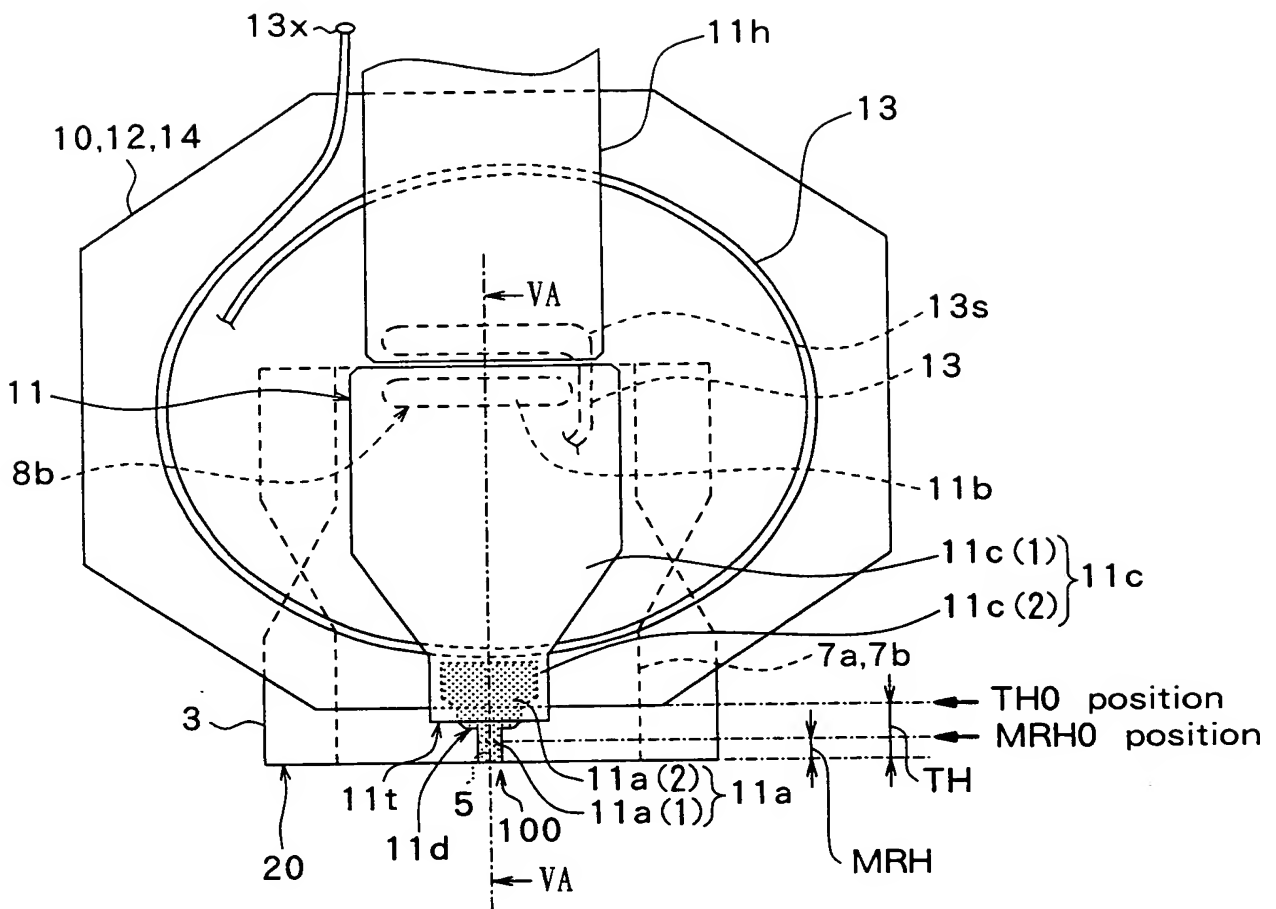


FIG.12

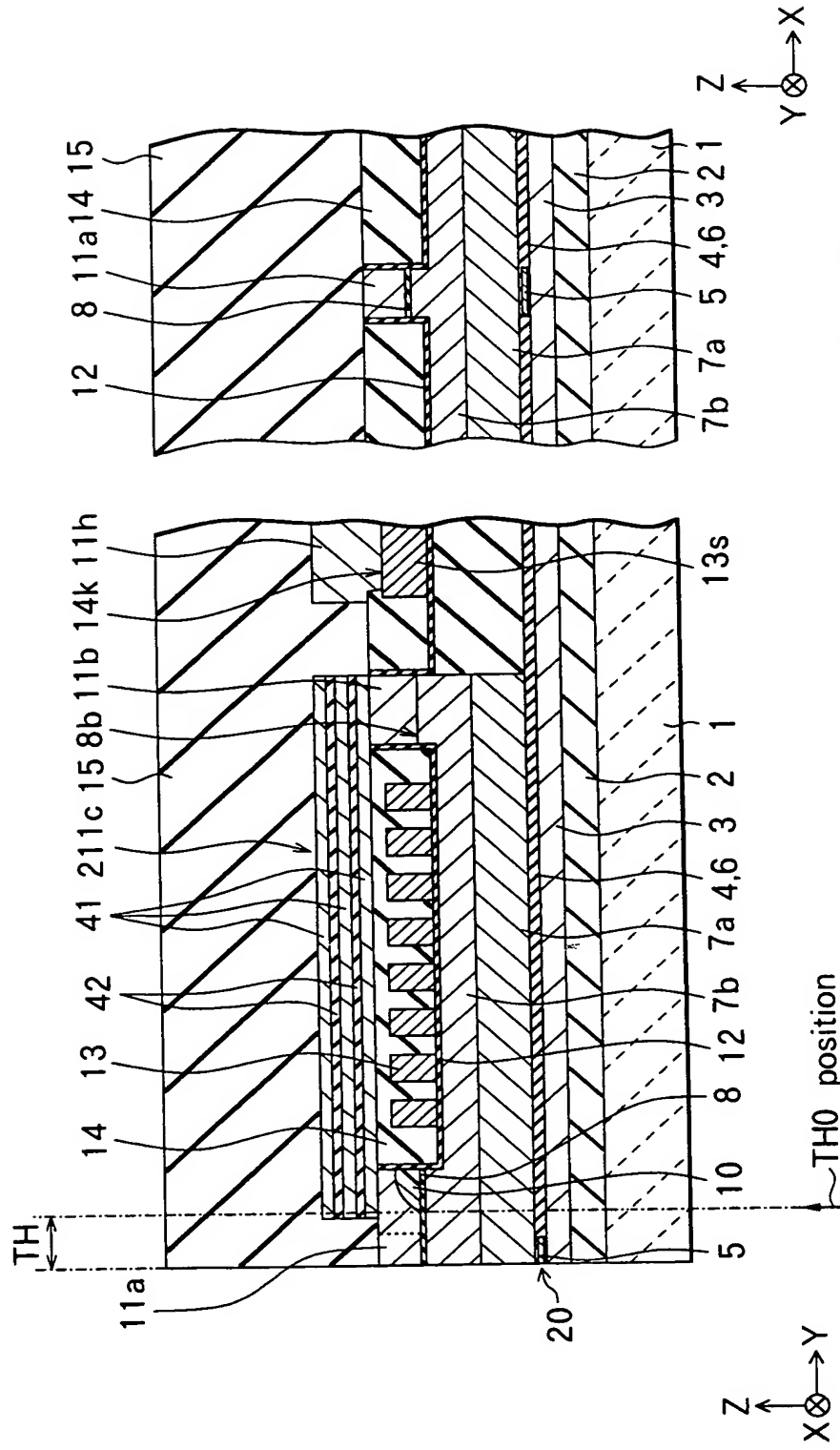


FIG.13B

FIG.13A

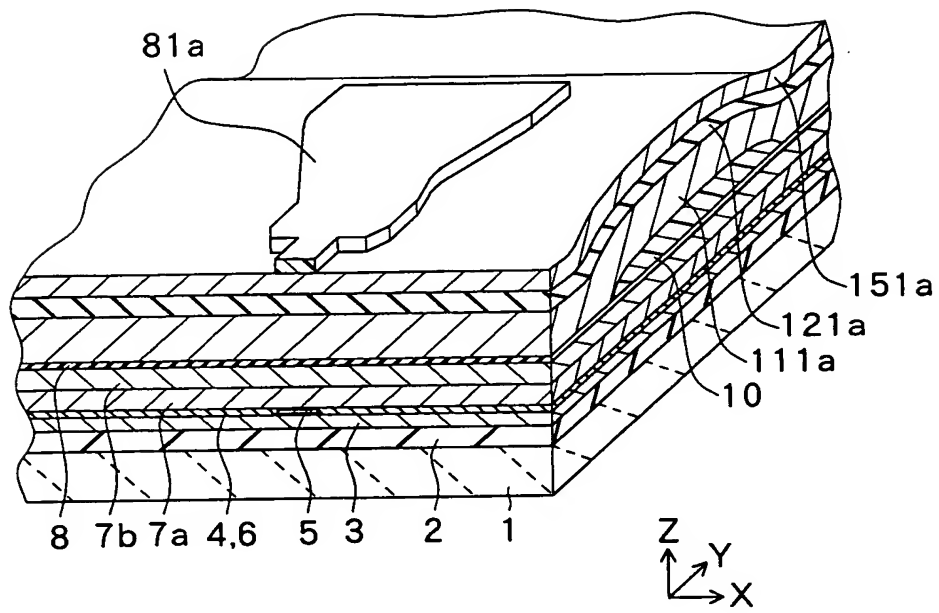


FIG.14

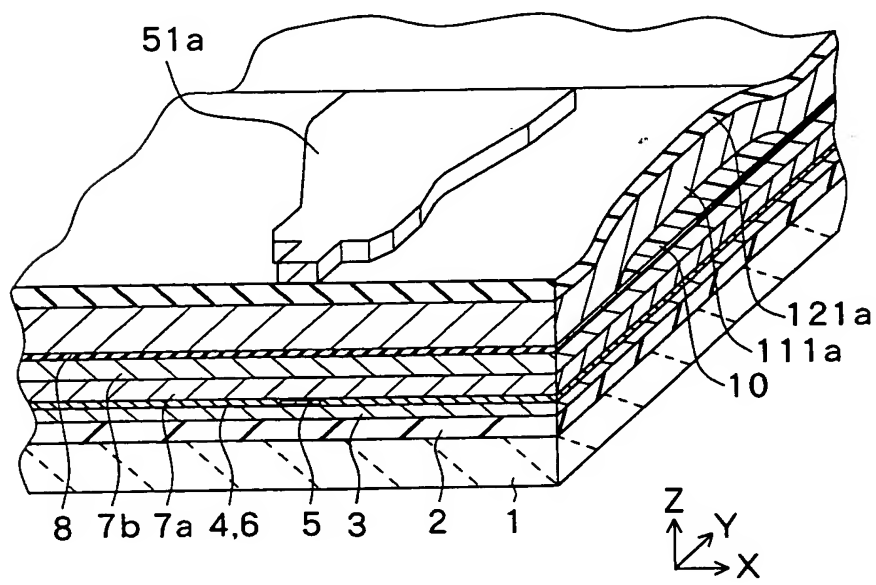


FIG.15

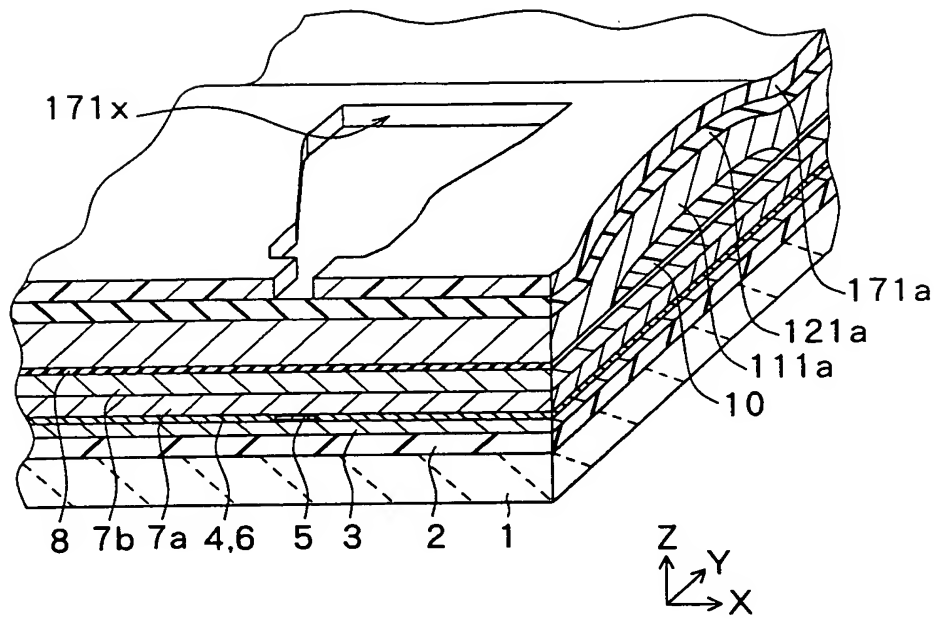


FIG. 16

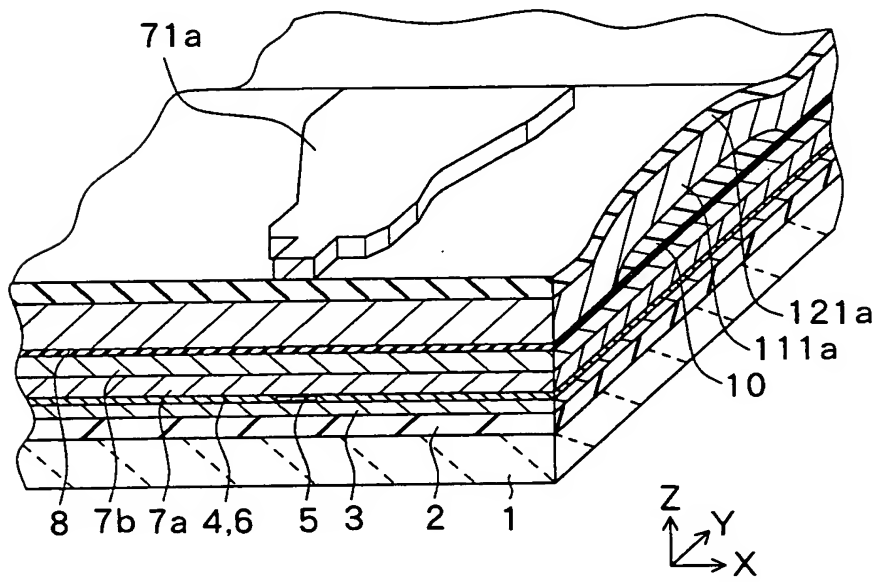


FIG. 17

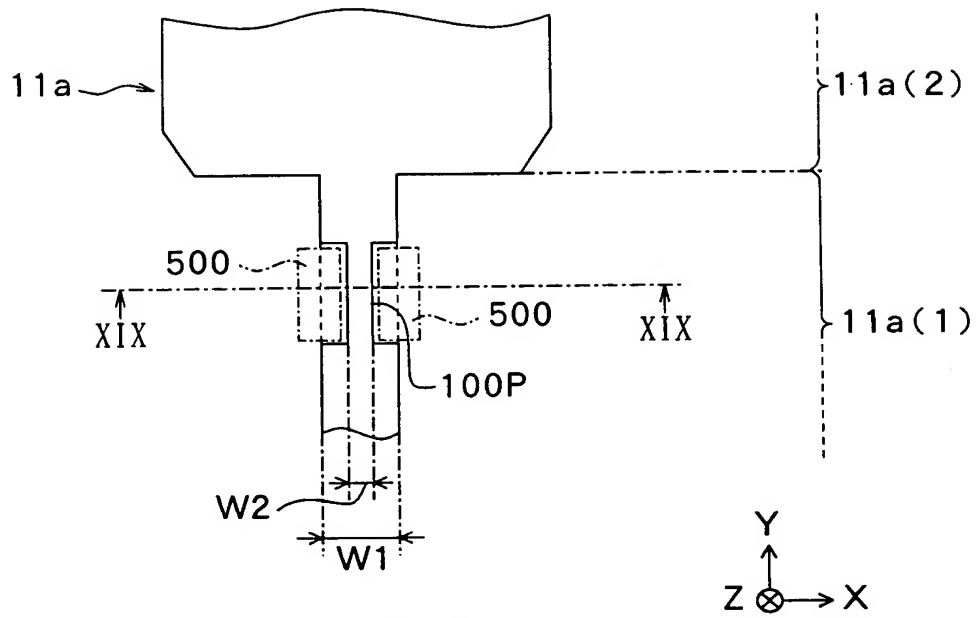


FIG. 18

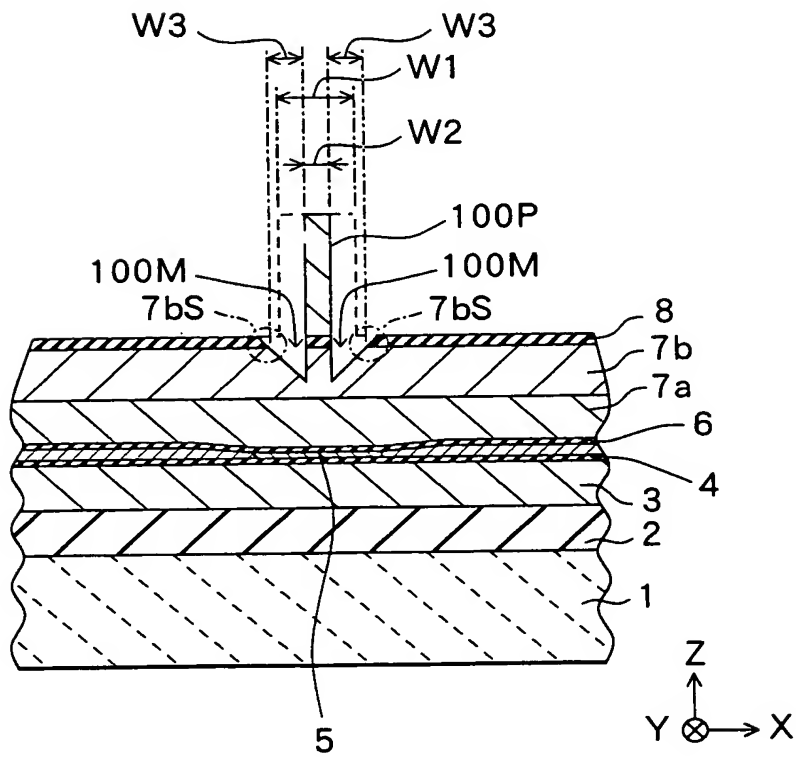


FIG. 19

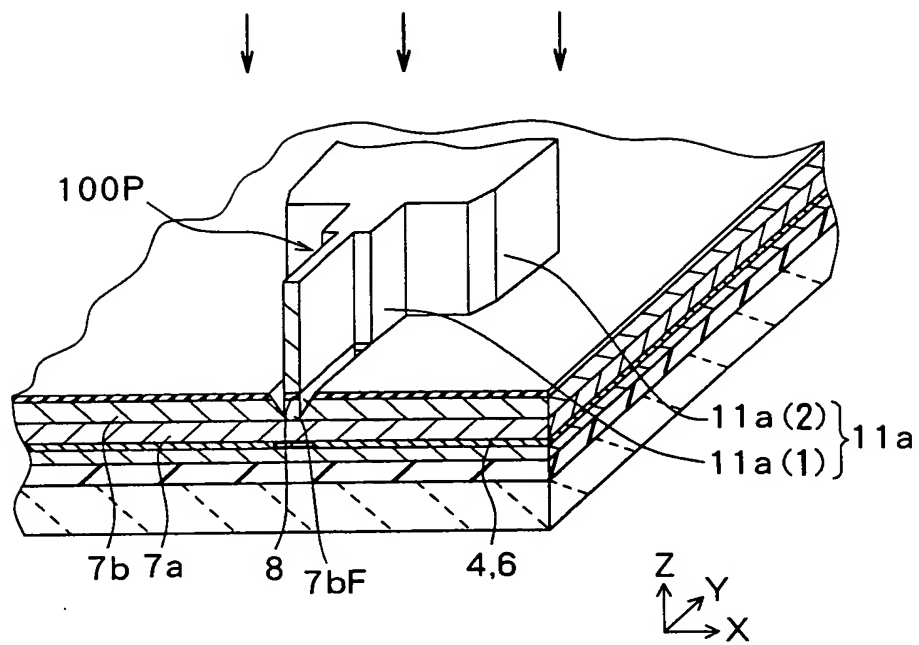


FIG.20

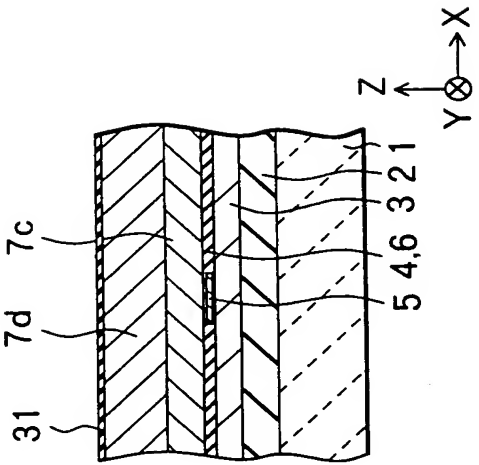


FIG.21B

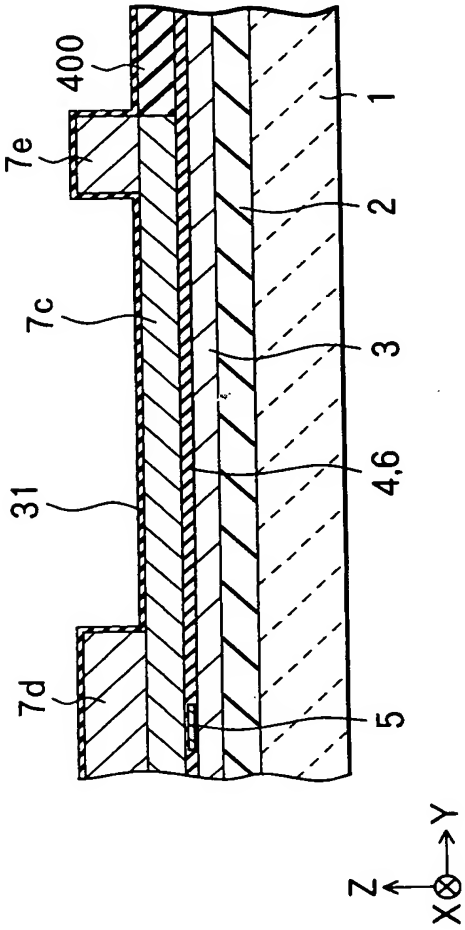


FIG.21A

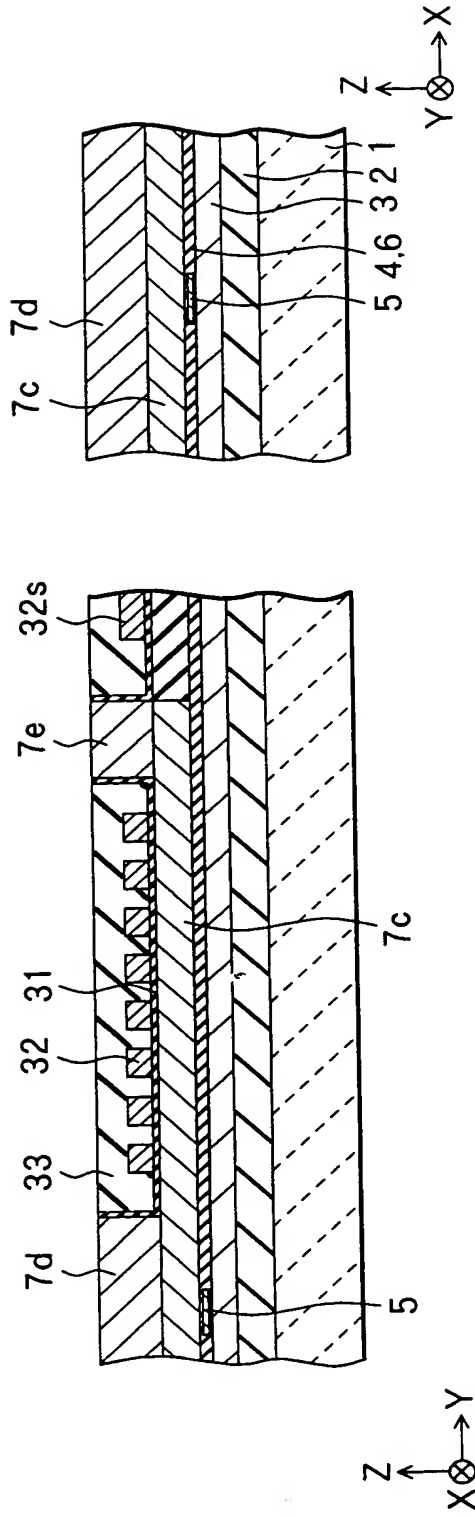


FIG. 22B

FIG. 22A

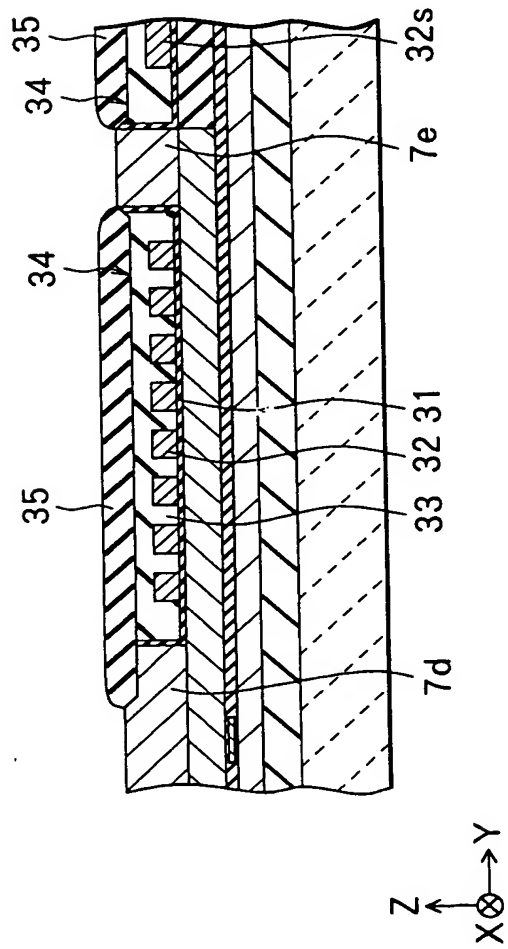


FIG.23A

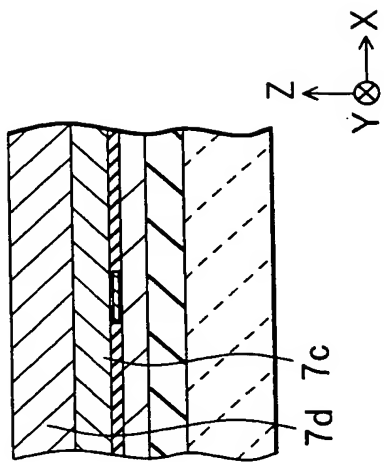


FIG.23B

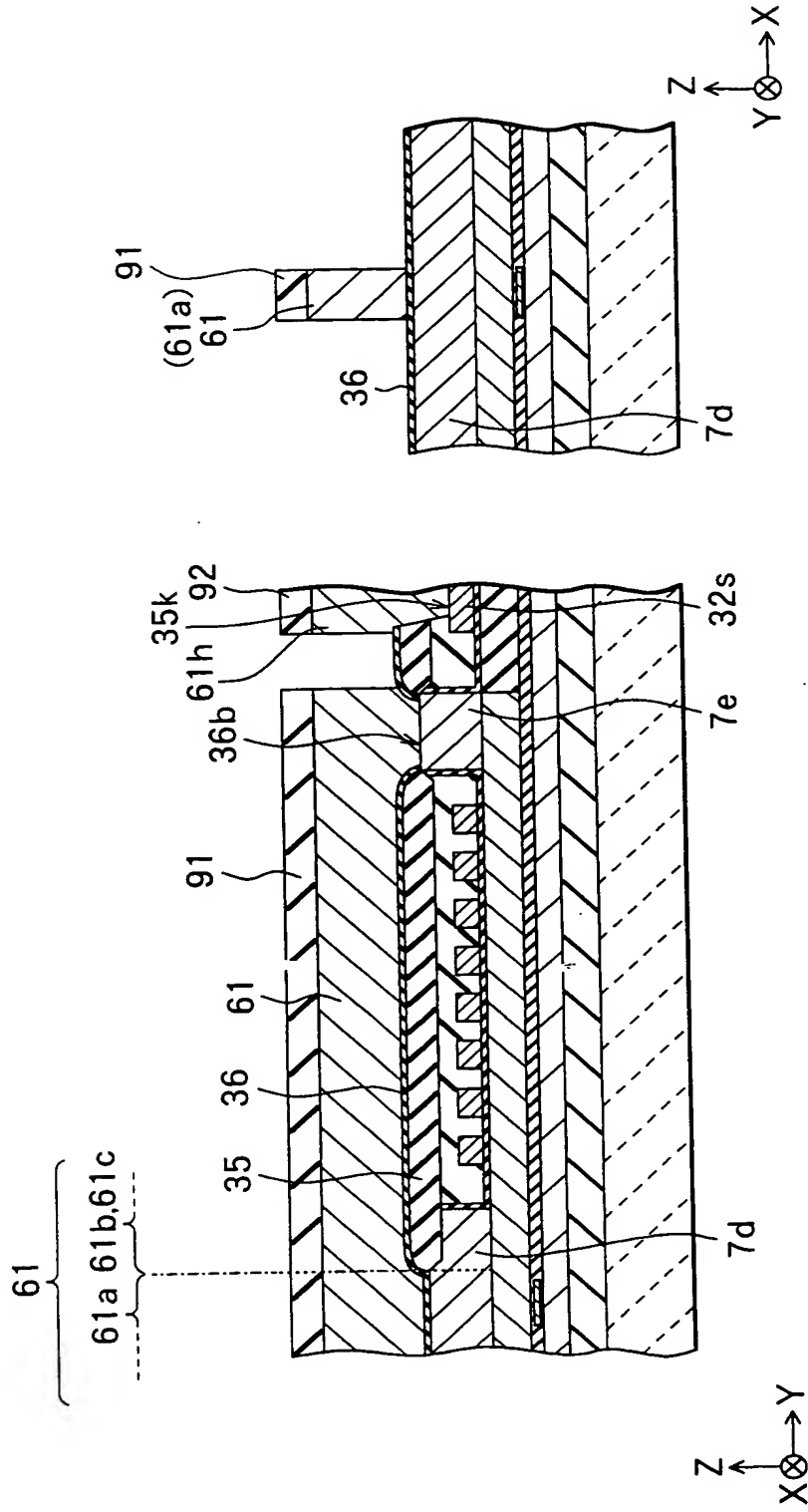
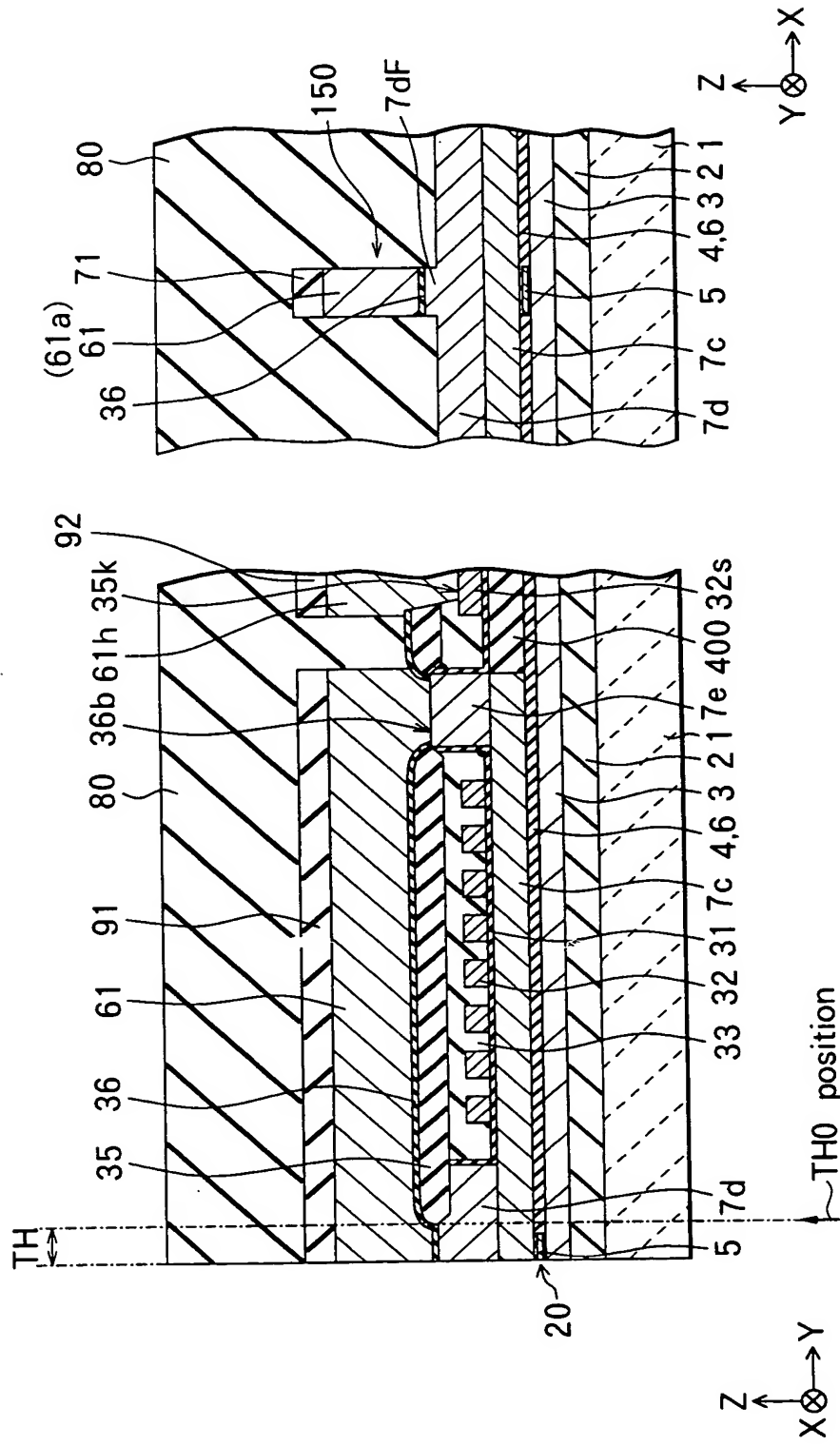


FIG.24B

FIG.24A



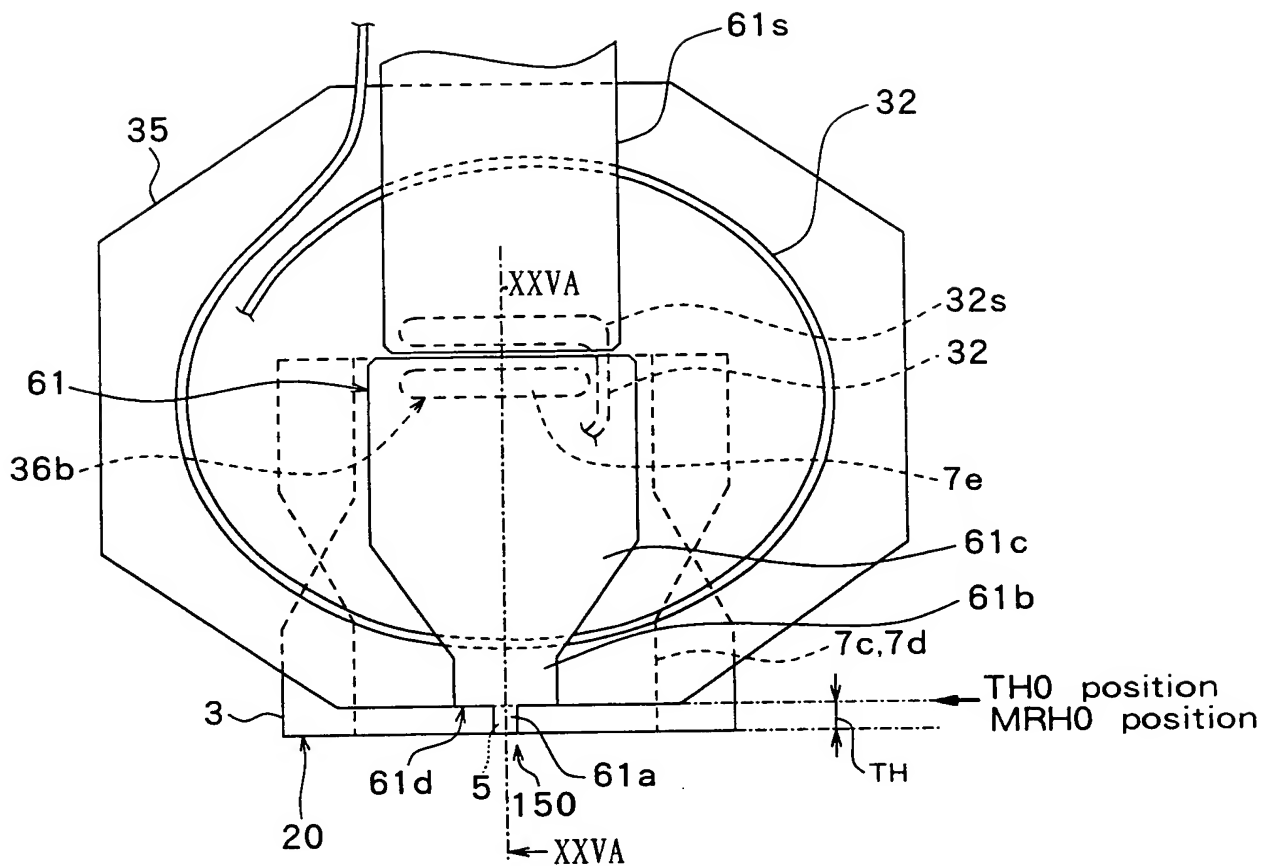


FIG.26

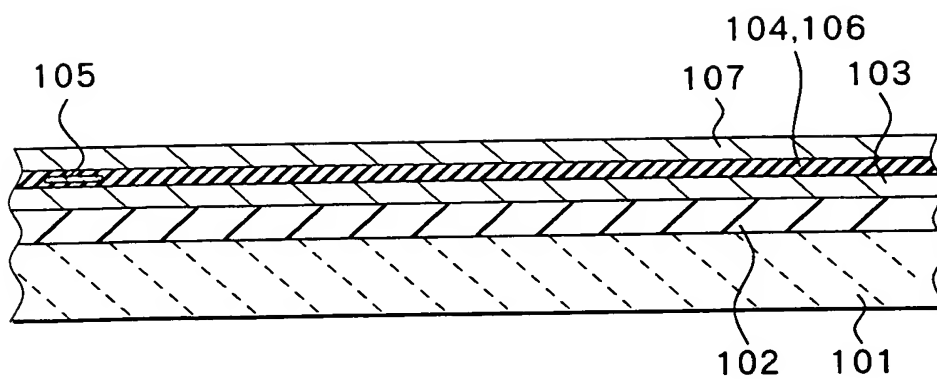


FIG.27
RELATED ART

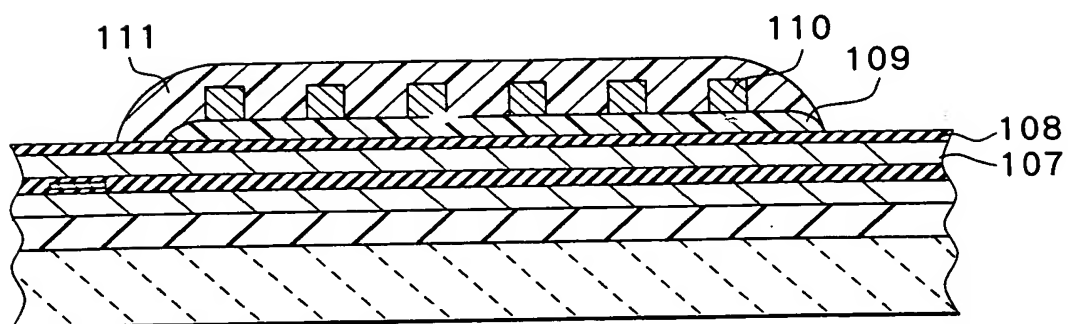


FIG.28
RELATED ART

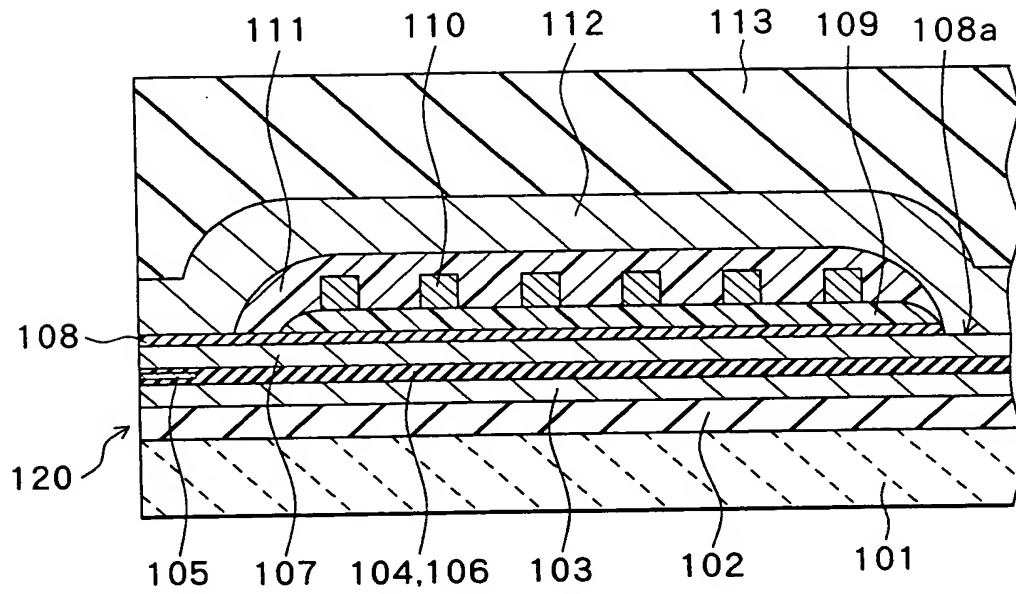


FIG.29
RELATED ART

Diagram illustrating a cross-sectional view of a semiconductor device. The device consists of a substrate (101) with multiple layers (102, 103, 104, 106, 107) and a patterned layer (108). A bracket (200) indicates a region of the patterned layer. Dimensions P2W and P2L are shown for the patterned layer. Labels 112(112b) and 121 are also present.

FIG.31
RELATED ART

FIG.32
RELATED ART

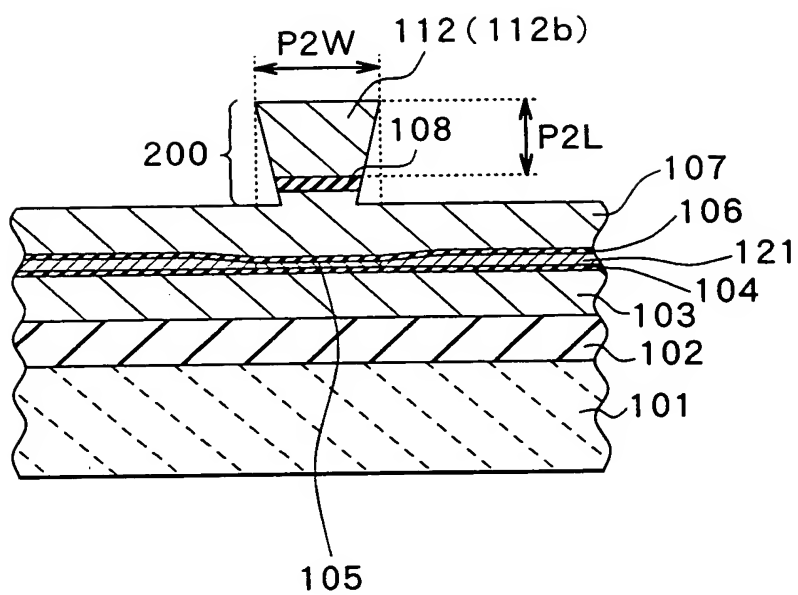


FIG.33
RELATED ART